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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,725	12/28/2000	James S. Burns	2207/10120	6772

23838 7590 10/07/2005

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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/749,725	BURNS ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2005 and 12 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10-15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4-8, 10-15, 17, and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

RD

DETAILED ACTION

1. Claims 1, 2, 4-8, 10-15, 17, and 18 have been examined. Claims 1, 4, 7, 10, 13, and 15 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed in 22 March 2005 and Amendment as filed on 12 July 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4-8, 10-15, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirata et al., U.S. Patent Number 5,430,851.

5. In regard to claim 1, Hirata et al. disclose a processor (col. 4, line 50), comprising:

a. A plurality of pipelined functional units for executing instructions (Fig. 3, elements 16-18);

b. A scheduler (Fig. 4, instruction setup units 34 and instruction schedule unit 35 [col. 9, lines 36-45]), coupled to the plurality of functional units (fig. 4, 16-18),

c. Wherein the scheduler is programmed to, in a first stage (fig. 4, instruction setup units 34 comprise of the first stage), map each of at least two separate instruction groups to at least a portion of the functional units independently of each other

(independent instruction setup units for each instruction stream [col. 5, lines 55-59] map instructions to functional units by setting a type tag T [col. 6, lines 19-20, 25-27]), and based at least in part on functional unit availability and instruction dependencies (signal R, col. 6, lines 54-56), perform a merging (col. 6, lines 11-14, instruction schedule unit merges the instructions from each of the instruction groups) and remapping of the at least two separate instruction groups to the at least a portion of the functional units (col. 8, lines 48-56, instruction schedule unit remaps the instructions based on resource conflicts) in a second stage (fig. 4, instruction schedule unit 35 comprises of a second stage)

6. In regard to claim 2, Hirata et al. further disclose that the scheduler is programmed to deliver the instruction to the portion of functional units following merging and remapping (instructions are sent to the functional units from the instruction schedule unit 35 which is responsible for the merging and remapping, fig. 4 and col. 8, 51-56).

7. In regard to claim 4, Hirata et al. further disclose that at least a portion of the functional units execute instructions from the at least two instruction groups (col. 5, 40-44; col. 6, 25-34).

8. In regard to claim 5, Hirata et al. further disclose that the instruction groups (instruction streams) follow a simultaneous multi-threading structure (col. 2, lines 65-68).

9. In regard to claim 6, Hirata et al. further disclose that the instruction groups are prioritized to prevent pipeline failures (resulting from contention) during execution of instructions (col. 7, 65-68; col. 8, 1-10).

10. In regard to claims 7 and 13, Hirata et al. disclose a method of dispersing instructions (instruction schedule unit distributes instructions to the functional units, col. 6, lines11-14) to be executed by a processor (col. 4, line 50), comprising:

a. In a first stage (instruction setup unit 34), map (instruction setup units [fig. 4, 34] map instructions to functional units by setting a type tag T [col. 6, lines 19-20, 25-27]) each of at least two separate instruction groups (instruction streams, col. 5, lines 55-59) to at least a portion of functional units independently of each other (instruction setup unit 34); and

b. Based at least in part on functional unit availability and instruction dependencies (signal R, col. 6, lines 54-56), perform a merging (col. 6, lines 11-14, instruction schedule unit merges the instructions from each of the instruction groups) and remapping (col. 8, lines 48-56, instruction schedule unit remaps the instructions based on resource conflicts) of the at least two separate instruction groups to the at least a portion of functional units (col. 9, lines 46-64: the instruction schedule unit 35 receives an instruction subgroup of up to 2 instructions from the instruction stream being fetched) in a second stage (instruction schedule unit 15).

11. In regard to claims 8 and 14, Hirata et al. further disclose the step of delivering the instructions to portions of functional units following merging and remapping (instructions are sent to the functional units from the instruction schedule unit which is responsible for the merging and remapping, fig. 4 and col. 8, 51-56).

12. In regard to claims 10 and 15, Hirata et al. further disclose at least a portion of the functional units execute instructions from the at least two instruction groups (col. 5, 40-44; col. 6, 25-34).

13. In regard to claims 11 and 17, Hirata et al. further disclose that the instruction groups (instruction streams) follow a simultaneous multi-threading structure (col. 2, lines 65-68).

14. In regard to claims 12 and 18, Hirata et al. further disclose that the instruction groups are prioritized to prevent pipeline failures (resulting from contention) during execution of instructions (col. 7, 65-68; col. 8, 1-10).

Response to Arguments

15. Applicant's arguments filed 12 July 2005 have been fully considered but they are not persuasive.

16. Applicant's argue in essence on pages 7-8 "...nothing in the disclosure of Hirata suggests an *independent* mapping of each instruction group in a first stage, and then a *merging* and *remapping* of the instruction groups in a second stage..." This has not been found persuasive. The claim language in the claim is similar to the previous claim language. The current claim language is just the previous claim language reorganized. As stated in the rejection above, Hirata teaches that the instruction setup units provide a first independent mapping between the instructions and the functional in column 5, lines 55-59 and column 6, lines 19-20 and 25-27. The instruction setup units provide a decoded instruction that includes an instruction type tag T that indicates a function execution unit (Hirata column 6, lines 19-34). The instructions are merged in the instruction schedule unit, since there is no distinction within this unit of which instruction was received from which instruction setup unit, so the decoded instructions are

treated as one larger group of instructions to be sent to the functional units (Hirata column 6, lines 11-16). Then, depending on signal R, which signals which functional units are free to accept new instructions (Hirata column 6, lines 54-56), the scheduler remaps the instructions to the correct functional units dependent on when the functional unit is free (Hirata column 8, lines 48-56).

17. Applicant's argue in essence on pages 7-8

> The independent mapping, merging and remapping performed by the claimed scheduler is described in more detail in the present specification...
>
> ...
>
> ...The merging and remapping may enable optimal use of functional units as described in the present specification, for example in the paragraph bridging pages 6 and 7 and the following exemplary scenarios.

18. This has not been found persuasive. This argument is unclear to the Examiner. It seems that the Applicant is relying on portions of the specification to show how the claims distinguish from the art, but it the Examiner is not clear which portions of the specification the Applicant is trying to use and it seems that the Applicant is relying upon features that have not been claimed. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
29 September 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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